Real-Time processing on configurable multimedia systems

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Xilinx
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Structure of the talk

• Next Generation Virtex 5 technology
• What is a real-time multimedia system
• MPEG4 decode example
• Programming reconfigurable systems
• Virtex 5 revisited in video terms
• Conclusions and future work
FPGAs Drive the Process

New process technology drives down cost
FPGAs can take advantage of new technology faster than ASICs and ASSPs

FPGA 2010: 32 nm, 5 Billion transistors

The cost of IC development increases. Therefore customers want to buy reconfigurable and programmable platforms, instead of developing their own.
65nm Process Technology

- 40-nm gate length (physical poly)
- 1.6nm oxide thickness (16 Angstrom)
  - ~5 atomic layers
- Triple-Oxide II technology
  - 3 oxide thicknesses for optimum power and performance
- 1.0 Vcc core
  - Lower dynamic power
- Mobility engineered transistors (strained silicon)
  - Maximum performance at lowest AC power

Over 1 Billion Transistors on a 23 x 23 mm Chip
LX Platform
Overview
Two Generations of ASMBL
(Application-Specific Modular BLock Architecture)

Virtex-4

Virtex-5
2\textsuperscript{nd} Generation of ASMBL

Easy to create sub-families

- **LX**: Logic + parallel I/O
- **LXT**: Logic + serial I/O
- **SXT**: DSP + serial I/O
- **FXT**: PPC + fastest serial I/O

Many choices to optimize cost and performance
Continuing the Drive for Innovation

- Advanced Configuration Options
- Most Advanced High-Performance Express Fabric
- 36Kbit Dual-Port Block RAM / FIFO with Integrated ECC
- SelectIO with ChipSync Technology and XCITE DCI
- Low-Power RocketI/O™ GTP Serial Transceivers*
- PCI-Express Endpoint Blocks*
- 10/100/1000 Mbps Ethernet MAC Blocks*
- 550 MHz Clock Management Tile with DCM and PLL
- 25x18 DSP Slice with Integrated ALU
- Integrated System Monitor

*LXT Platform Only*
A multi-media system

2 streams of 720p MPEG4 decode

Xilinx University Program, www.xilinx.com/univ XUPv2p board
Real-Time systems

• Meet specific guarantees:
  – e.g. 2 MPEG4 decode streams at 30fps, 720p
  – No buffer problems
  – No pixels missing, no drop back to previous frame

• Throughput guarantees:
  – e.g. Input streams: 2 streams of max 8Mbit/s
  – e.g. runs over 54Mbit/s wireless infrastructure

• Working system allows measurements, e.g. average core power of $1.5V \times 0.74\,\text{A} = 1.11\,\text{Watt}$
MPEG4 development
MPEG4 Development steps

• MPEG committee standards program, hard to read C
• System model of the functions with a partitioning along the architecture for the selected profile
• Performance and throughput analysis
• Hand written VDHL
• Performance and throughput analysis
• Driver for High Level Synthesis methodology
Implicit Flow control

Buffer
• full and empty signals, asynchronous behavior

Shared memory
• scheduled access guarantees proper order

Programming concepts: blocking read or writes, blocking guards (CSP), network of actors.
MPEG-4 Simple Profile Decoder
MPEG-4 Simple Profile Decoder

FPGA 0/1

MPEG-4 SP Decoder

External SRAM 1

Memory Controller

Copy Controller

Shared Memory

Display Controller

External SRAM 2

System Interface

Input Interface

Processing

Input Interface

Motion

Parser/VLD

FIFO

Object FIFO

Motion Vectors

Inverse Scan

Inverse Quantisation / IDCT

8×8 Block

Object FIFO

DCT Coeff

Texture/IDCT

Copy Controller

Controller

Display Controller

Memory Controller

Shared Memory

FIFO

External SRAM 2

External SRAM 1

System Interface

Input Interface

Processing

Processing

Processing

Processing

FIFO 8

FIFO

FIFO

FIFO
MPEG-4 Simple Profile Decoder

Diagram showing the architecture of an MPEG-4 Simple Profile Decoder with various components such as motion compensation, parser, and memory organization.
MPEG-4 Decoder - Resources
(Throughput of 108 kMacroblks/sec)

<table>
<thead>
<tr>
<th>Hardware Block</th>
<th>Lines C</th>
<th>Lines VHDL</th>
<th>BRAMs</th>
<th>Slices</th>
<th>MULTs</th>
</tr>
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<tr>
<td>Input Interface</td>
<td>430</td>
<td>100</td>
<td>1</td>
<td>20</td>
<td>0</td>
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<tr>
<td>Parser/VLD</td>
<td>1,891</td>
<td>5,820</td>
<td>0</td>
<td>1,670</td>
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<tr>
<td>Copy Controller</td>
<td>406</td>
<td>1,634</td>
<td>0</td>
<td>700</td>
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<tr>
<td>Motion Compensation</td>
<td>265</td>
<td>1,527</td>
<td>0</td>
<td>500</td>
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<tr>
<td>Texture/IDCT</td>
<td>943</td>
<td>2,969</td>
<td>6</td>
<td>2,050</td>
<td>23</td>
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<tr>
<td>Texture Update</td>
<td>126</td>
<td>401</td>
<td>0</td>
<td>150</td>
<td>2</td>
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<tr>
<td>Auxiliary Controllers</td>
<td>189</td>
<td>1,916</td>
<td>16</td>
<td>1,470</td>
<td>0</td>
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<tr>
<td>Communication/Memory</td>
<td>0</td>
<td>0</td>
<td>28</td>
<td>250</td>
<td>0</td>
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<tr>
<td><strong>Total</strong></td>
<td>4,250</td>
<td>14,367</td>
<td>51</td>
<td>6,810</td>
<td>30</td>
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</table>
MPEG-4 Decoder: Macro Statistics
(extracted from XST report)

- Large, diverse design with varying data widths and macro types
- Notes: Registers listed as 1-bit elements; 304 multipliers in design
MPEG-4 Decoder: Resources

Estimated FPGA Resources of Various Macro Types

- Registers
- Adders/Subtractors
- Counters
- Comparators
- Multiplexers
- Distributed Memory
- Miscellaneous

Total Elements (Estimated)

LUTs

FPGA Resources

Registers
MPEG-4 SP Decoder

- Sample analysis of 55k MB/sec design extrapolated from Mobile CIF @ 500 kbps
Video Decoder Activity Diagram

- Initial diagram identified unbalanced pipelines
- Pipelining of Texture/IDCT provided 1.72x throughput improvement
MPEG-4 Simple Profile Decoder

Abstract from FPGA details or Processor Details
Refactor the Memory Hierarchy

- currently rec
- previously rec

→ only 1 frame
→ update only changed MBs
→ enables burst copies
→ enables multiple streams

bufferY/U/V

searchArea
Virtex-5 LX
8 MPEG4 decoders

<table>
<thead>
<tr>
<th>Category</th>
<th>Virtex-4</th>
<th>Virtex-5</th>
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<tbody>
<tr>
<td>Tools</td>
<td>XST/ISE 8.1.02i</td>
<td>XST/ISE 8.2i</td>
</tr>
<tr>
<td>Devices</td>
<td>XC4VFX140-11</td>
<td>Virtex5 part</td>
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</tbody>
</table>
8 Decoders: Resources

- 35% fewer LUTs
- Dramatic improvements for multiplexers, memory, and misc. logic
- Same VHDL source code used for both designs

Estimated FPGA Resources for Eight MPEG-4 Decoder Design

<table>
<thead>
<tr>
<th>Design Resources</th>
<th>Virtex-4</th>
<th>Virtex-5</th>
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<tbody>
<tr>
<td>Registers</td>
<td>21,248</td>
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<tr>
<td>LUTs</td>
<td>67,523</td>
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<td>BlockRAMs</td>
<td>233</td>
<td>233</td>
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<tr>
<td>DSP Elements</td>
<td>192</td>
<td>216</td>
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</tbody>
</table>

Diff. = 6932
Logic Synthesis-Driven Results

- Synthesis uses 6-input LUTs efficiently: fewer logic levels
- 23% increase in synthesized frequency, from 95MHz to 117MHz
- From 720p to 1080p video standards with little effort
# Virtex-5 LXT Platform

<table>
<thead>
<tr>
<th></th>
<th>5VLX30T</th>
<th>5VLX50T</th>
<th>5VLX85T</th>
<th>5VLX110T</th>
<th>5VLX220T</th>
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<tbody>
<tr>
<td>Logic Cells</td>
<td>30,720</td>
<td>46,080</td>
<td>82,944</td>
<td>110,592</td>
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<td>LUT6/Flip-Flops</td>
<td>19,200</td>
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<td>69,120</td>
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<tr>
<td>Total Distributed RAM (Kbits)</td>
<td>320</td>
<td>480</td>
<td>840</td>
<td>1,120</td>
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<tr>
<td>Total Block RAM (Kbits)</td>
<td>1,296</td>
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<td>RocketIO GTP Channels</td>
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<td>10/100/1000 EMACs</td>
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</tbody>
</table>

X,Y  X = SelectIO, Y=RocketIO Channels

Estimedia workshop in the ESweek, 2006, korea, slide 29
Conclusions

• FPGA technology is moving extremely rapidly
• Complete connectivity + Multimedia systems can be build with reconfigurable technology
• Reconfigurable systems include the synthesis of the memory hierarchy
• Raising the programming level of abstraction for Real-Time reconfigurable systems include:
  – mapping from a high level of abstraction: networks of actors
  – building systems that can guarantee real-time behavior: new theory, new methods, new tools